

Data sheet acquired from Harris Semiconductor SCHS027C – Revised February 2004

# **CMOS Counter/Dividers**

High-Voltage Types (20-Volt Rating) CD4017B-Decade Counter with

10 Decoded Outputs

#### CD4022B-Octal Counter with

8 Decoded Outputs

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■ CD4017B and CD4022B are 5stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high-speed operation, 2-input decode-gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the CD4017B or every 8 clock input cycles in the CD4022B and is used to ripple-clock the succeeding device in a multi-device counting chain.

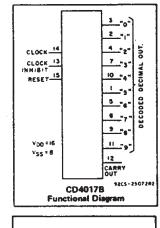
### Features:

- Fully static operation
- Medium-speed operation . . .
- 10 MHz (typ.) at V<sub>DD</sub> = 10 V Standardized symmetrical out
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

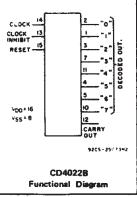
#### Applications:

- Decade counter/decimal decode display (CD4017B)
- Binary counter/decoder
- Frequency division
- Counter control/timers
- Divide-by-N counting
- For further application information, see ICAN-6166 "COS/MOS MSI Counter and Register Design and Applications"

The CD4017B and CD4022B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic package (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4017B types also are supplied in 16-lead small-outline packages (M and M96 suffixes).



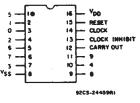
**CD4017B, CD4022B Types** 



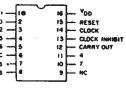
**RECOMMENDED OPERATING CONDITIONS** 

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	V <sub>DD</sub>	LIN	AITS	UNITS
	(V)	Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package- Temperature Range)		3	18	v
Clock Input Frequency, f <sub>CL</sub>	5 10 15	1   1	2.5 5 5.5	MHz
Clock Pulse Width, t <sub>W</sub>	5 10 15	200 90 60		. ns
Clock Rise & Fall Time, t <sub>rCL</sub> , t <sub>fCL</sub>	5 10 15	UNLIN	NITED*	14.
Clock Inhibit Setup Time, t <sub>s</sub>	5 10 15	230 100 70	-	ns
Reset Pulse Width, t <sub>RW</sub>	5 10 15	260 110 60		ns
Reset Removal Time, t <sub>rem</sub>	5 10 15	400 280 150		ns



TOP VIEW CD4017B TERMINAL DIAGRAM



92C5-24464AI

TOP VIEW NC - no connection CO4022B TERMINAL DIAGRAM

\*Only if Pin 14 is used as the clock input. If Pin 13 is used as the clock input and Pin 14 is tied high (for advancing count on negative transition of the clock), rise and fall time should be  $\leq$  15  $\mu$ s.

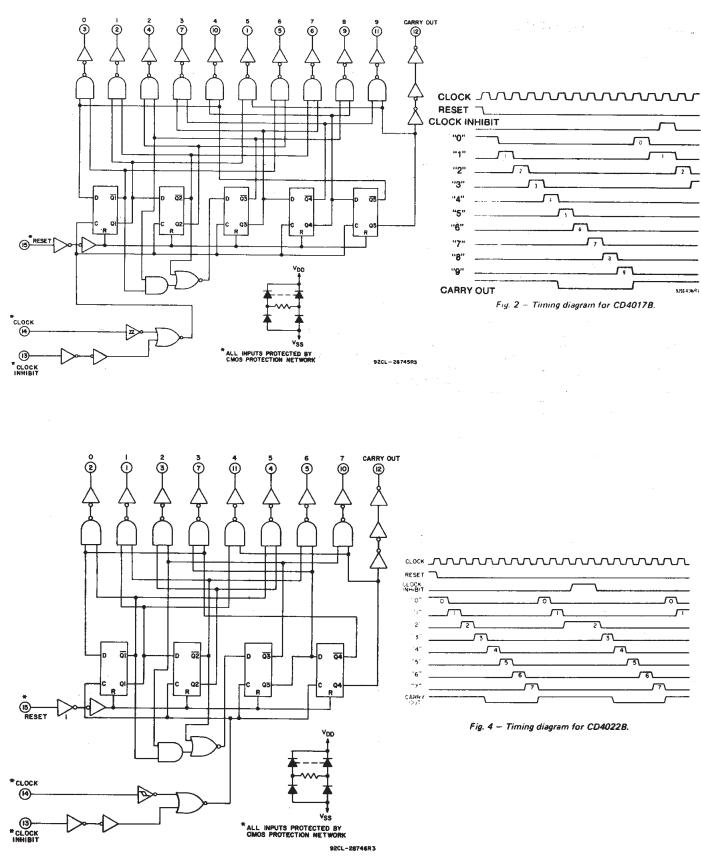
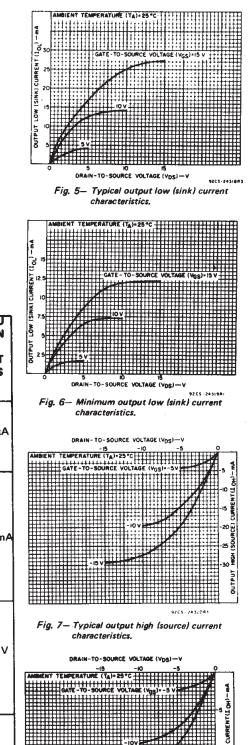


Fig. 3 – Logic diagram for CD4022B.

MAXIMUM RATINGS, Absolute-Maximum Values:	
DC SUPPLY-VOLTAGE RANGE, (VDD)	
Voltages referenced to V <sub>SS</sub> Terminal)	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V <sub>DD</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (PD):	
For $T_A = -55^{\circ}C$ to $+100^{\circ}C$	
For TA = +100°C to +125°C DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T <sub>A</sub> = +100°C to +125°C DEVICE DISSIPATION PER OUTPUT TRANSISTOR	. Derate Linearity at 12mW/ <sup>o</sup> C to 200mW
For $T_A = +100^{\circ}C$ to $+125^{\circ}C$ . DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A = FULL$ PACKAGE-TEMPERATURE RANGE (All Packag OPERATING-TEMPERATURE RANGE ( $T_A$ ).	. Derate Linearity at 12mW/°C to 200mW e Types)
For $T_A = +100^{\circ}C$ to $+125^{\circ}C$ . DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A = FULL$ PACKAGE-TEMPERATURE RANGE (All Packag OPERATING-TEMPERATURE RANGE ( $T_A$ ).	. Derate Linearity at 12mW/°C to 200mW e Types)
For $T_A = +100^{\circ}C$ to $+125^{\circ}C$ DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR $T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package)$	. Derate Linearity at 12mW/°C to 200mW e Types)



3

COMMERCIAL CMOS HIGH VOLTAGE ICs

HIGH (SOURCE)

OUTPUT

- Minimum output high (source) current

characteristics.

# STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC		DITIO			LIMITS AT INDICATED TEMPERATURES (°C)						U N I T
	V <sub>0</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	55	40	+85	+125	Min.	+25 Typ.	Max.	S
	_	0,5	5	5	5	150	150	_	0.04	5	,
Quiescent Device	-	0,10	10	10	10	300	300	-	0.04	10	uА
Current,	-	0,15	15	20	20	600	600	_	0.04	20	
IDD Max.	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	
(Sink) Current	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
IOL Min.	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	0.51	-1	-	m۸
(Source)	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
Current,	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
OH WIT	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage:		0,5	5		0	_	0	0.05			
Low-Level,		0,10	10		0	.05		-	0	0.05	
VOL Max.	-	0,15	15		0	.05		-	0	0.05	l v
Output	-	0,5	5		4	.95		4.95	5	_	
Voltage: High-Level,		0,10	10		9	.95		9.95	10		
VOH Min.	-	0,15	15		14	.95		14.95	15	· _	
Input Low	0.5,4.5	-	5			1.5		-	-	1.5	
Voltage	1,9	_	10			3			-	3	
VIL Max.	1. <b>5,13.5</b>	_	15			4			_	4	V
Input High	0.5,4.5	-	5			3.5		3.5	-	-	
Voltage,	1,9	-	10			7		7	-	·	
V <sub>IH</sub> Min.	1.5,13.5	-	15			11		11	-	-	
Input Current IN Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 <sup>-5</sup>	±0.1	μΑ

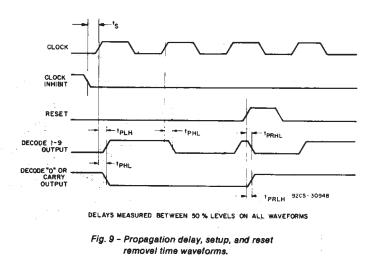
Fig. 8

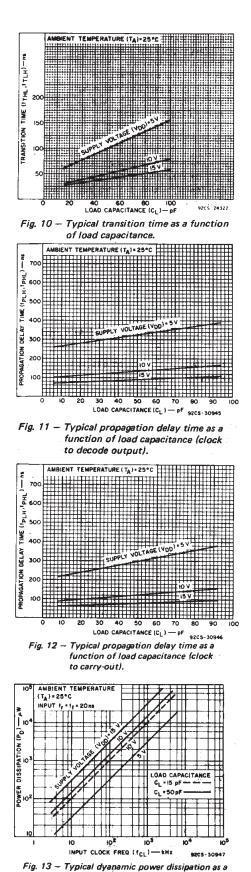
### DYNAMIC ELECTRICAL CHARACTERISTICS

At T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 k $\Omega$ 

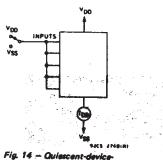
CHARACTERISTIC	CONDITIONS		UNITS		
-	V <sub>DD</sub> (V)	Min.	Тур.	Max.	
CLOCKED OPERATION		•	<b>-</b>	•	·
	5	_	325	650	
Propagation Delay Time, tpHL, tpLH	10	-	135	270	
Decode Out	15	-	85	170	ns
	5	-	300	600	
Carry Out	10	. <u>-</u> .	125	250	
	15	_	80	160	
Transition Time, tTHL, tTLH	5	-	100	200	
Carry Out or Decode Out Line	10	-	50	100	ns
	15	_	40	80	
	5	2.5	5	-	
Maximum Clock Input Frequency, fCL*	10	5	10	-	MHz
	15	5.5	11	-	
	5	_	100	200	
Minimum Clock Pulse Width, tw	10	-	45	90	ns
	15		30	60	
Clock Rise or Fall Time, t <sub>r</sub> CL, t <sub>f</sub> CL	5, 10, 15		IMITE	D	
Minimum Clock Inhibit	5		115	230	
to Clock Setup Time, t <sub>s</sub>	10	_	50	100	ns
	15	_	35	70	
Input Capacitance, CIN	Any Input	-	5	_	pF
RESET OPERATION	······································			<b>-</b>	
Propagation Delay Time, tPHL, tPLH	5	_	265	530	
Carry Out or Decode Out Lines	10	_	115	230	ns
	15	-	85 <sup>.</sup>	170	
· · · · · · · · · · · · · · · · · · ·	5	_	130	260	
Minimum Reset Pulse Width, tw	10	-	55	110	ns
	15	-	30	60	
	5		200	400	,
Ainimum Reset Removal Time	10			280	ns
	15		75	150	

\* Measured with respect to carry output line.

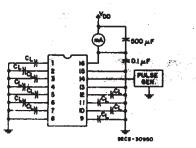




function of clock input frequency.



rig. 14 - Quiescent-devicecurrent test circuit.



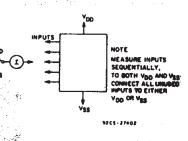
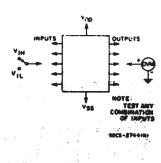


Fig. 15 -- Input-leekage current.

CLOCK CL

Fig. 17 - Dynamic power dissipation test circuit.

Fig. 18 – Divide by N counter (N  $\leq$  10) with N decoded outputs.



#### Fig. 16 - Input-voltage test circuit.

When the Nth decoded output is reached (Nth clock pulse) the S-R flip flop (constructed from two NOR gates of the CD4001B) generates a reset pulse which clears the CD4017B or CD4022B to its zero count. At this time, if the Nth decoded output is greater than or equal to 6 in the CD-4017B or 5 in the CD4022B, the COUT line goes high to clock the next CD4017B or CD-4022B counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output low resets the S-R flip flop to enable the CD4017B or CD4022B. If the Nth decoded output is less than 6 (CO4017B) or 5 (CD4022B), the COUT line will not go high and, therefore, cannot be used. in this case "0" decoded output may be used to perform the clocking function for the next counter.

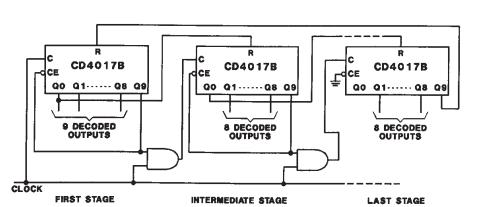
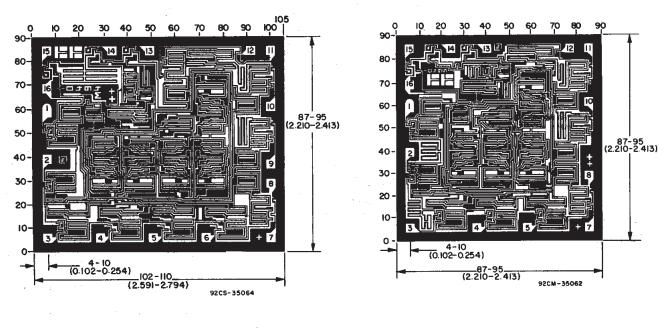


Fig. 19 - Cascading the CD4017B.

### CHIP DIMENSIONS AND PAD LAYOUTS



CD4017BH

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CD4022BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).



10-Jun-2014

## PACKAGING INFORMATION

Orderable Device		Package Type	Package Drawing	Pins			Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
89270AKB3T	(1) OBSOLETE		Drawing	0	Qty	(2) TBD	(6) Call TI	(3) Call TI	-55 to 125	(4/5)	
CD4017BE	ACTIVE	PDIP	N	16	25	Pb-Free	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4017BE	
CD4017BE	ACTIVE	FDIF	IN	10	25	(RoHS)	CONFDAU	N/Aloi Pkg Type	-5510125	CD4017BE	Samples
CD4017BEE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4017BE	Samples
CD4017BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4017BF	Samples
CD4017BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4017BF3A	Samples
CD4017BF3AS2534	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI			
CD4017BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4017BM	Samples
CD4017BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4017BM	Samples
CD4017BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4017BM	Samples
CD4017BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4017BM	Samples
CD4017BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4017B	Samples
CD4017BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4017B	Samples
CD4017BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM017B	Samples
CD4017BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM017B	Samples
CD4017BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM017B	Samples
CD4017BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM017B	Samples
CD4022BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4022BE	Samples
CD4022BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4022BE	Samples



# PACKAGE OPTION ADDENDUM

10-Jun-2014

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CD4022BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4022BF	Samples
CD4022BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4022BF3A	Samples
CD4022BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4022B	Samples
CD4022BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4022B	Samples
CD4022BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM022B	Samples
CD4022BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM022B	Samples
CD4022BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM022B	Samples
CD4022BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM022B	Samples
CD4022BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM022B	Samples
JM38510/05651BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05651BEA	Samples
M38510/05651BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 05651BEA	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)



#### www.ti.com

10-Jun-2014

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF CD4017B, CD4017B-MIL, CD4022B, CD4022B-MIL :

• Catalog: CD4017B, CD4022B

• Military: CD4017B-MIL, CD4022B-MIL

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

www.ti.com

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

TEXAS INSTRUMENTS





### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION	

\*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4017BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4017BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4017BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4022BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4022BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TEXAS INSTRUMENTS

www.ti.com

# PACKAGE MATERIALS INFORMATION

14-Jul-2012



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4017BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4017BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4017BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD4022BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4022BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/E 08/12

# D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) –16x0,55 -14x1,27 -14x1,27 16x1,50 5,40 5.40 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60 .55 Example 1. Solder Mask Opening (See Note E) -0,07 All Around

NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  $\beta$ . This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## MECHANICAL DATA

## PLASTIC SMALL-OUTLINE PACKAGE

### 0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 $\bigcirc$ Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS \*\* 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G\*\*)

**14-PINS SHOWN** 

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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